FUTEK
ADVANCED SENSOR TECHNOLOGY, INC.

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Tel: (949) 465-0900
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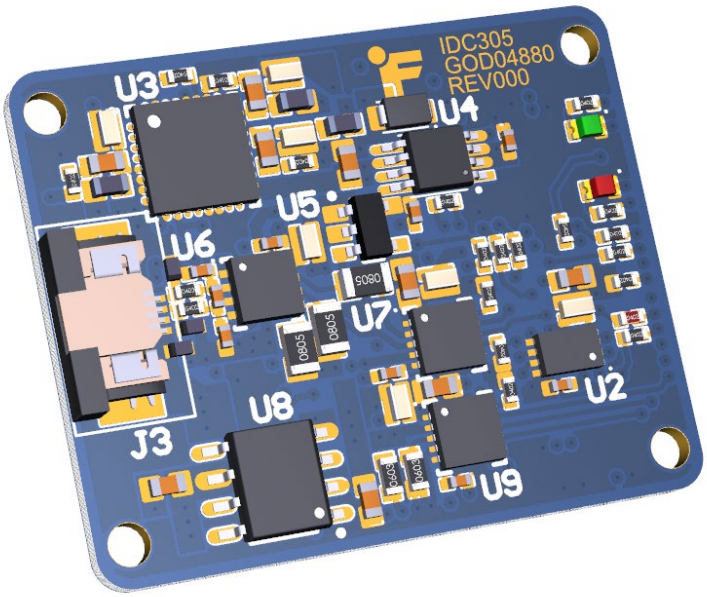
IDC305 SPI Communication



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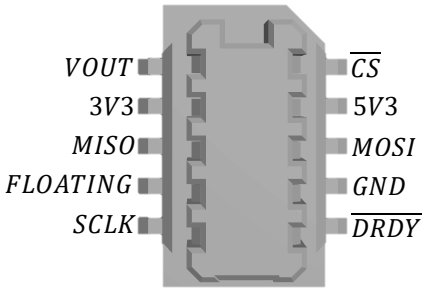
Note: Firmware Version 3

The current version of this document (EM1026-F) applies to Firmware Version 3 only and communicates with the standalone app.

1. SPI Connections:

1.1 Pin Out



1.2 Pin Descriptions

1.2.1 $MISO$: Master in slave out
1.2.2 $SCLK$: Serial clock
1.2.3 $\overline{CS}$: Active low chip select. ***Do not drive the $\overline{CS}$ line low until the device has booted up completely. The Red LED turns off once the board has booted and is ready to communicate. This process takes 3 seconds. Also ensure that the $\overline{CS}$ line is not driven low unless the $\overline{DRDY}$ is also low.***
1.2.4 $MOSI$: Master out slave in
1.2.5 $\overline{DRDY}$: This pin is used to keep all communication synchronized. It notifies the master device when new data from the sampling system is ready to ensure that the master is always collecting the latest data. When the $\overline{DRDY}$ pin goes low it indicates that the data is ready. This pin can be used to externally interrupt the master. The pin returns high when the system is in a conversion state and returns low once new data is ready. The pin does *not* return high once data is read—it wil *only* return high once the system enters a conversion state.

2. Communication

2.1 Configuration

2.1.1 SPI Clock Speed: Tested at 5MHz, 6.25MHz, 8.33MHz, and 12.5 MHz
2.1.2 SPI Mode: CPOL: 0 CPHA: 0 (MODE 0)

2.2 Packet Structure

2.2.1 Command Send

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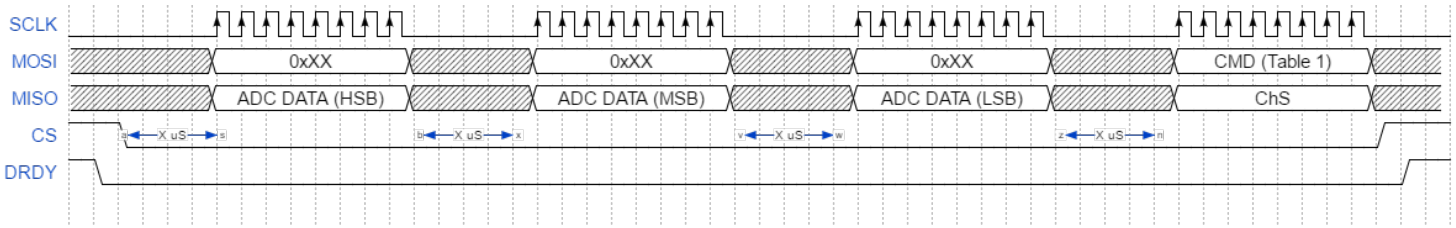
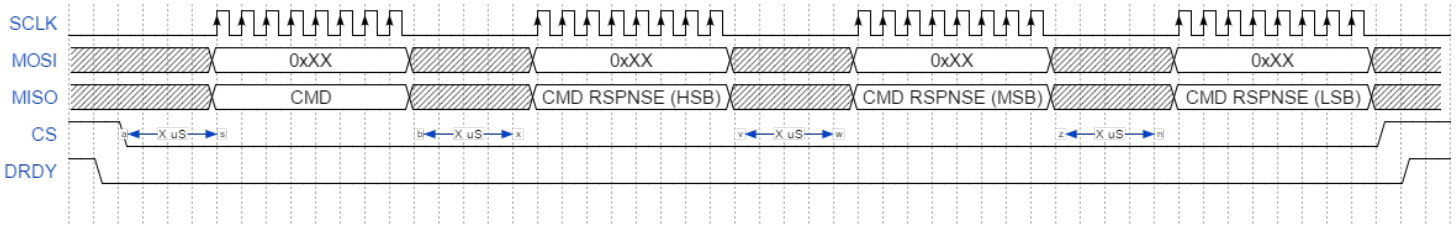
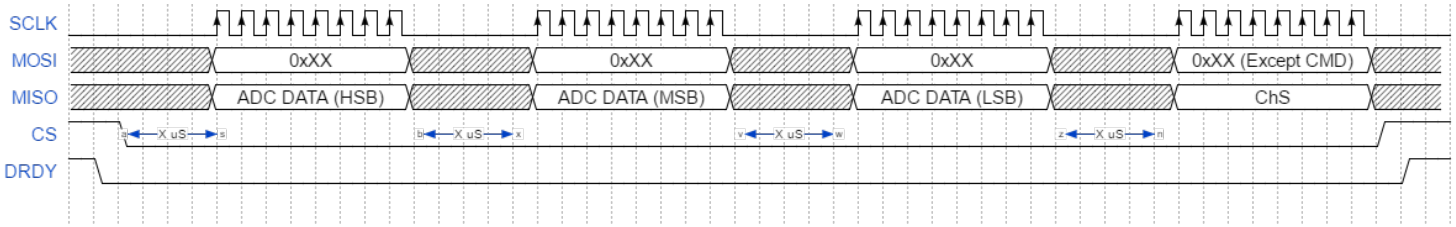


2.2.2 Command Response (Must be read in the next DRDY low period after sending a command)



2.2.3 ADC Read



2.2.4 Data Integrity and Validity

Last byte <ChS> gives the checksum of the first three bytes
<HSB> <MSB> <LSB> <ChS>

Ex. Let's assume:
HSB = 0x0A
MSB = 0x0B
LSB = 0x0C

Then ChS will be calculated and sent as follows:
ChS = (0x0A * 1) + (0x0B * 2) + (0x0C * 3) = 0x44

In this case the received packet from the IDC305 would be:
<0x0A> <0x0B> <0x0C> <0x44>

If the ChS calculation exceeds one byte it will only send the LSB.

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Ex. Let's assume: ChS = 0x2FD, which includes two bytes, it will then be sent as ChS = 0xFD.

***NOTE: 0xXX = Don't Care**
****NOTE: X uS = no delay or any delay as long as all 4 bytes are transferred prior to DRDY going high**

Fig.1 SPI Timing and Communication Structure (32-bits)

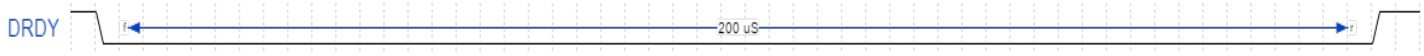

Fig.2 $\overline{\text{DRDY}}$ Period

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2.3 Command Set

Table.1 Command Definitions

COMMAND	DESCRIPTION	1st COMMAND BYTE
RCWCALNZ	Read Clockwise Calibration Natural Zero	0x0A
RCWCALP1	Read Clockwise Calibration Point One	0x0B
RCWCALP2	Read Clockwise Calibration Point Two	0x0C
RCWCALP3	Read Clockwise Calibration Point Three	0x0D
RCWCALP4	Read Clockwise Calibration Point Four	0x0E
RCWCALP5 (Positive Span)	Read Clockwise Calibration Point Five (Span)	0x0F
RCCWCALP1	Read Counter Clockwise Calibration Point One	0xB0
RCCWCALP2	Read Counter Clockwise Calibration Point Two	0xC0
RCCWCALP3	Read Counter Clockwise Calibration Point Three	0xD0
RCCWCALP4	Read Counter Clockwise Calibration Point Four	0xE0
RCCWCALP5 (Negative Span)	Read Counter Clockwise Calibration Point Five (Span)	0xF0
RFSSN	Read FUTEK Sensor Serial Number	0xBB
RIAC	Read Internal Activation Code	0xCC
RFRN	Read Firmware Revision Number	0xDD
RECHV	Read EEPROM Checksum Value	(Not Implemented)

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3. Power Supplies

3.1 Sequencing

3.1.1 All supplies (3.3V and 5.3V) must come in within 3 seconds of each other for the unit to function properly.

4. Indication

4.1 Red LED:

4.1.1 The red LED stays on until the device is ready to communicate. If this LED is on, do not communicate with the device.